IN THE CLAIMS:

1. (currently amended) For use in a wide-issue processor, a mechanism for identifying and tracking conditional ~~conditionally executing~~ instructions, comprising:

a conditional execution block state machine that tags and generates link pointers for instructions located in a conditional execution block; and

conditional link pointer registers, associated with stages in a pipeline of said processor, that contain and cause said link pointers to move therethrough as said instructions located in said conditional execution block move through said stages.

2. (original) The mechanism as recited in Claim 1 further comprising a conditional execution marking queue, associated with said conditional execution block state machine, that contains ones of said link pointers prior to storage in said conditional link pointer registers.

3. (original) The mechanism as recited in Claim 2 wherein said conditional execution marking queue is a five-bit, six-entry queue and comprises a reordering multiplexer.

4. (original) The mechanism as recited in Claim 1 further comprising a conditional execution attribute register, associated with a group stage of said pipeline, that contains an attribute associated with one of said conditional instructions.

5. (original) The mechanism as recited in Claim 4 wherein said conditional execution attribute register is a seven-bit register.

6. (original) The mechanism as recited in Claim 4 further comprising a conditional execution attribute queue that contains attributes read from said conditional execution attribute register.

7. (original) The mechanism as recited in Claim 6 wherein said conditional execution attribute queue is of variable depth and comprises a selecting multiplexer.

8. (currently amended) For use in a wide-issue processor, a method of identifying and tracking conditional ~~conditionally executing~~ instructions, comprising:

generating tags and link pointers for instructions located in a conditional execution block; and

causing said link pointers to move through conditional link pointer registers, associated with stages in a pipeline of said processor, as said instructions located in said conditional execution block move through said stages.

9. (original) The method as recited in Claim 8 further comprising containing ones of said link pointers in a conditional execution marking queue prior to storage in said conditional link pointer registers.

10. (original) The method as recited in Claim 9 wherein said conditional execution marking queue is a five-bit, six-entry queue and comprises a reordering multiplexer.

11. (original) The method as recited in Claim 8 further comprising containing an attribute associated with one of said conditional instructions in a conditional execution attribute register.

12. (original) The method as recited in Claim 11 wherein said conditional execution attribute register is a seven-bit register.

13. (original) The method as recited in Claim 11 further comprising containing attributes read from said conditional execution attribute register in a conditional execution attribute queue.

14. (original) The method as recited in Claim 13 wherein said conditional execution attribute queue is of variable depth and comprises a selecting multiplexer.

15. (original) A wide-issue digital signal processor (DSP), comprising:

a pipeline having stages capable of executing instructions conditionally;

a wide-issue instruction issue unit;

a conditional execution block state machine, associated with said instruction issue unit, that tags and generates link pointers for instructions located in a conditional execution block; and

conditional link pointer registers, associated with stages in a pipeline of said processor, that contain and cause said link pointers to move therethrough as said instructions located in said conditional execution block move through said stages.

16. (original) The DSP as recited in Claim 15 further comprising a conditional execution marking queue, associated with said conditional execution block state machine, that contains ones of said link pointers prior to storage in said conditional link pointer registers.

17. (original) The DSP as recited in Claim 16 wherein said conditional execution marking queue is a five-bit, six-entry queue and comprises a reordering multiplexer.

18. (original) The DSP as recited in Claim 15 further comprising a conditional execution attribute register, associated with a group stage of said pipeline, that contains an attribute associated with one of said conditional instructions.

19. (original) The DSP as recited in Claim 18 wherein said conditional execution attribute register is a seven-bit register.

20. (original) The DSP as recited in Claim 18 further comprising a conditional execution attribute queue that contains attributes read from said conditional execution attribute register.

21. (original) The DSP as recited in Claim 20 wherein said conditional execution attribute queue is of variable depth and comprises a selecting multiplexer.